Damir Gazizullin

437-328-4804 | dgazizul@uwaterloo.ca | linkedin.com/in/dgazizullin | github.com/sathworld | damirg.com

Education

University of Waterloo — Waterloo, ON

Candidate for Bachelor of Applied Science (B.A.Sc.), Electrical Engineering; GPA: 3.99 — *September 2022 – Present*

First in Class — *Fall 2022 (1A), Spring 2023 (1B), Winter 2024 (2A), Fall 2024(2B)*

Technical Skills

ECAD/Tools: Vivado, cocotb, PSpice, Verilator, Altium Designer, KiCad, ESPIDF, Git, STM32CubeMX, Docker
Languages: Verilog, SystemVerilog, C++, C, Python, Tcl, MATLAB
Lab Equipment: Oscilloscope, Logic Analyzer, Spectral Analyzer, DMM, Hot Air Station, Soldering Iron
Certifications: IPC Certified Interconnect Designer (CID)

Experience

Strivonix — Kitchener, ON

Product Development Coop — *January 2025 – April 2025*

- Led the design and testing of a portable pneumatic massage device's main 4-layer PCB, exceeding the required targets, achieving 97% functionality on the first design iteration and reducing BOM cost by over 30%
- Built ESP32-S3 firmware using ESP-IDF with FreeRTOS, utilizing software FSMs for peripheral interactions, achieving 95% accuracy for sensor readings using adaptively tuned Kalman filtering
- Implemented BLE drivers for the device to enable user-defined protocols that are saved in non-volatile memory (NVS)

UWASIC – IEEE SSCS Student Chapter — Waterloo, ON

Founder & Technical Lead — *December 2024 – Present*

- Founded and led UWASIC, which became the IEEE Solid-State Circuits Society Student Chapter for the KW Section
- Directed Dino Game ASIC project that targets open-source PDKs (IHP Open130-G2, SkyWater SKY130), reduced used area by over 10%, led RTL design and integration, meeting the tapeout deadline ahead of schedule by 1 week
- Achieved timing closure on the design, yielding 15% of extra slack time in both PDKs using OpenSTA
- Built custom simulator/visualizer using Verilator and C++ to debug pipeline and FSM behavior issues pre-layout
- Developed the onboarding project for an SPI-connected PWM Output Expander in Verilog, recruiting 50+ members
- Implemented a 5-bit-operand mixed-signal matrix-vector multiplier that outperforms digital-only designs in area by 25%

Electrium Mobility — Waterloo, ON

Electrical Team Lead — *December 2023 – Present*

- Taught 20+ workshops on schematic capture, PCB layout and routing, board bring-up, as well as IPC-compliant design and soldering, improving the reliability of the submitted designs by 30%
- Designed and validated the design of a custom brushless motor electronic speed controller (ESC), reducing cost by 20% and extending the number of available IO by 10% compared to existing micromobility ESCs on the market

Projects

Custom 8-bit Computer Tape-Out | ***Verilog, Python, Verilator, cocotb*** — September 2024 – December 2024

- Architected custom 8-bit RISC ISA with 16 instructions to balance datapath simplicity and opcode density
- Designed and verified pipelined ALU and register file blocks in Verilog, simulated with Verilator and cocotb
- Integrated modules from multiple teams to produce tapeout-ready GDS with >20% area savings
- Validated timing with post-layout netlists and RC extraction to ensure functional accuracy

Wearable Telehealth Device | ***C++, MATLAB, ThingSpeak, Blynk API*** — August 2022 – January 2023

- Built a WiFi-enabled wearable using ESP8266 and 5 I2C sensors for biometric monitoring
- Implemented ECG signal processing in MATLAB, achieving >95% arrhythmia classification accuracy
- Created mobile dashboard with Blynk API and ThingSpeak for cloud monitoring and alerts